WDDD 2006 -- CALL FOR PAPERS

Workshop on Duplicating, Deconstructing, and Debunking

http://www.ece.wisc.edu/~wddd

Boston, Massachusetts
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Held in conjunction with the 33rd Intl. Symposium on Computer Architecture (ISCA-33)

Organizers:

- Bryan Black, Intel Labs
  bryan.black@intel.com
- Harold Cain, IBM Research
  tcain@us.ibm.com

Important Deadlines

Abstract due:	April 7, 2006
Submission:	April 14, 2006
Acceptance:	April 28, 2006
Final version:	May 19, 2006

Program Committee:

- Mauricio Breternitz, Intel
- Doug Burger, UT-Austin
- Mikko Lipasti, Wisconsin
- Gabriel Loh, Georgia Tech
- Ken Lueh, Intel
- Yale Patt, UT-Austin
- Ryan Rakvic, US Naval Academy
- Mauricio Serrano, IBM Research

Workshop Overview:

WDDD provides the computer systems research community a forum for work that validates or duplicates earlier results; deconstructs prior findings by providing greater, in-depth insight into causal relationships or correlations; or debunks earlier findings by describing precisely how and why proposed techniques fail where earlier successes were claimed, or succeed where failure was reported.

Traditionally, computer systems research conferences have focused almost exclusively on novelty and performance, neglecting an abundance of interesting work that lacks one or both of these attributes. A significant part of research—in fact, the backbone of the scientific method—involves independent validation of existing work and the exploration of strange ideas that never pan out. This workshop provides a venue for disseminating such work in our community. Published validation experiments strengthen existing work, while thorough comparisons provide new dimensions and perspectives. Studies that refute or correct existing work also strengthen the research community, by ensuring that published material is technically correct and has sound assumptions. Publishing negative or strange or unexpected results will allow future researchers to learn the hard lessons of others, without repeating their effort.

This workshop will set a high scientific standard for such experiments, and will require insightful analysis to justify all conclusions. The workshop will favor submissions that provide meaningful insights and point to underlying root causes for the failure or success of the technique under investigation. Acceptable work must thoroughly investigate and clearly communicate why the proposed technique performs as the results indicate. Rebuttals may be invited for debunking submissions.

Submission Topics:

- Independent validation of earlier results with meaningful analysis
- In-depth analysis and sensitivity studies that provide further insight into earlier findings, or identify key parameters or assumptions that affect the results
- Studies that refute earlier findings, with clear justification and explanation
- Negative results for ideas that intuitively make sense and should work, along with explanations for why they do not

Workshop Scope:

Computer Architecture	**Code Generation and Optimization**
Processor architecture/microarchitecture	Feedback-driven optimization
Memory hierarchy	Phase-based optimization
Multiprocessor systems	Modulo/trace scheduling
Power-efficient architectures	Efficient profiling techniques
Dependable architectures	Binary translation/optimization
Compiler/architecture interaction	Compilion support for thread-level speculation
Application-specific, reconfigurable and embedded architectures	Dynamic compilation, adaptive/continuous optimization