

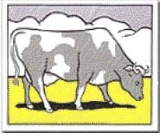
Precise and Accurate Processor Simulation

Harold Cain, Kevin Lepak,
Brandon Schwartz, and

Mikko H. Lipasti

University of Wisconsin—Madison

<http://www.ece.wisc.edu/~pharm>

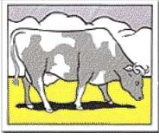


Architecture Research?

*Genius is one percent inspiration and
ninety-nine percent perspiration.*

--Thomas Edison

- This is not a talk about inspiration
 - No new ideas or gimmicks
- This is a talk about perspiration
 - Mostly graduate student perspiration
- Infrastructure, tools, methodology
[CAECW Talk/Paper, February 2002]

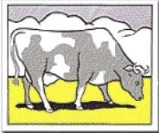


Performance Modeling

- Analytical models
- Queuing models
- Simulation
 - Trace-driven
 - **Execution-driven**
 - Full system
- Why?

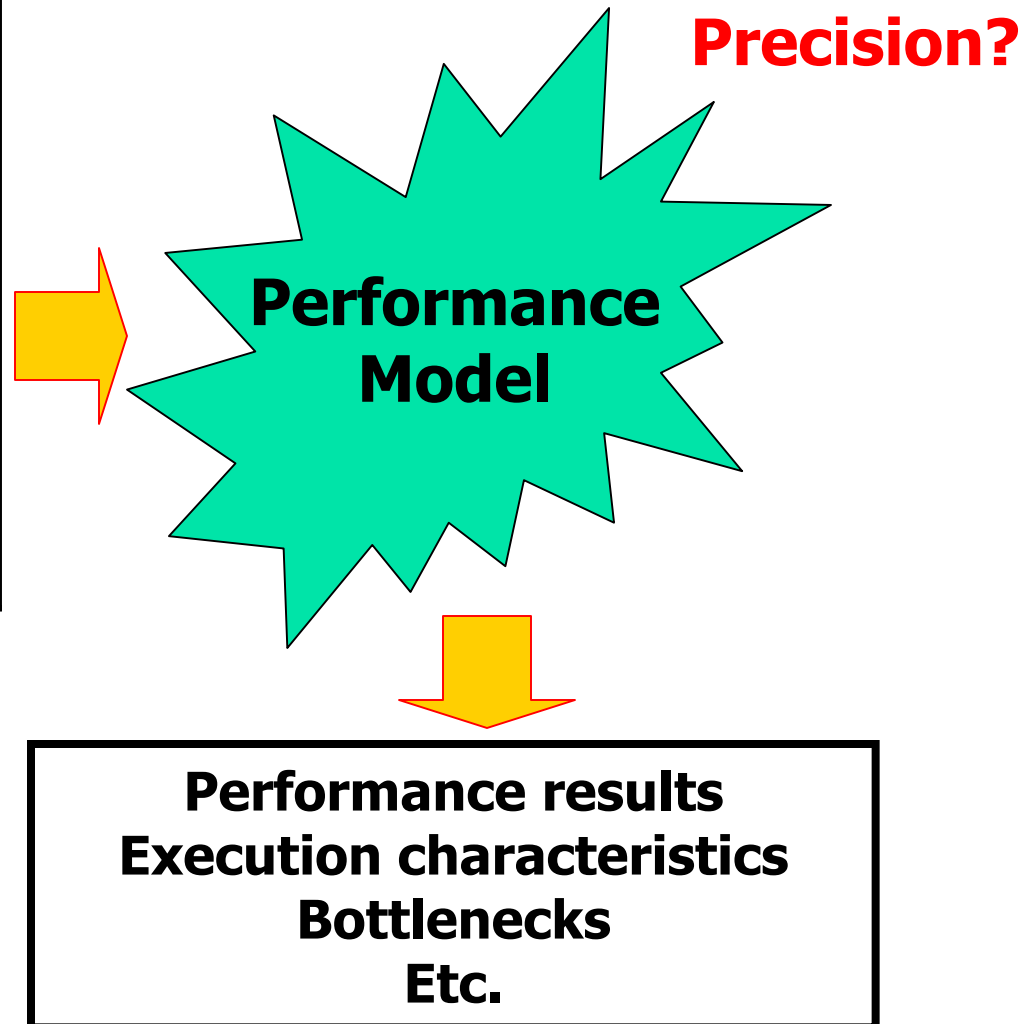
**Most widely
used in
academic
research**

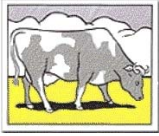
Perceived accuracy and precision



Performance Modeling

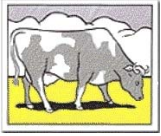
Inputs
Program Characteristics -instruction mix, miss rates
Execution Trace -instruction, address, both
Program binary + input sets
Operating system, program(s), etc.





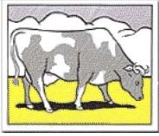
Talk Outline

- *Introduction & Motivation*
 - *Performance Modeling*
- Precision, Accuracy, Flexibility
- PharmSim Overview
- Causes of Inaccuracy
 - O/S Effects
 - Coherent I/O (DMA)
 - Wrong-path Effects
- Summary & Conclusions

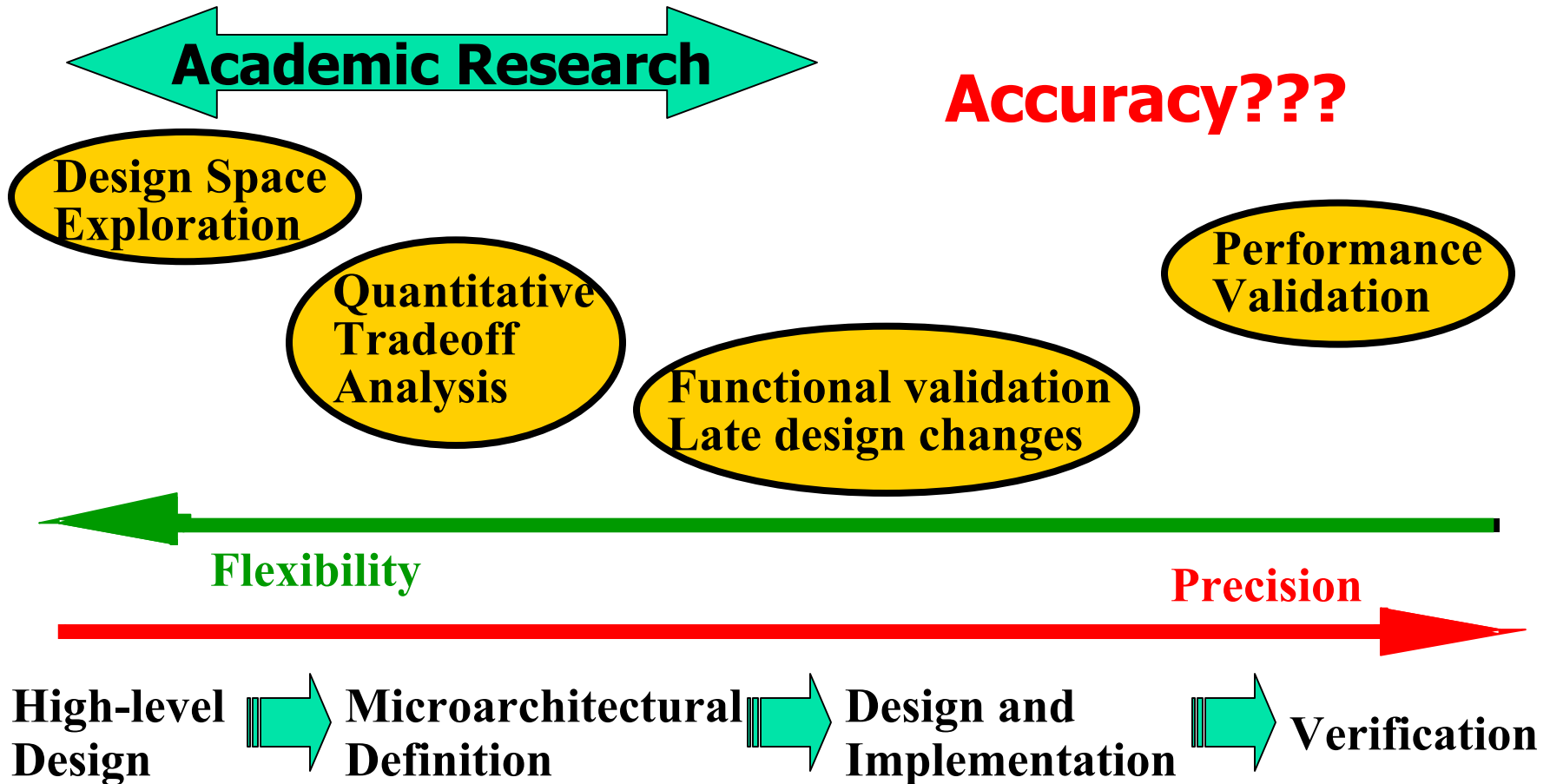


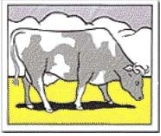
Precision, Accuracy, Flexibility

- Precision
 - How closely simulator matches design
 - Latency, bandwidth, resource occupancy, etc.
- Accuracy
 - How closely simulation matches reality
 - Requires precision
 - Also requires replication of real-world conditions, inputs
- Flexibility?
 - Enables exploration of broad design space



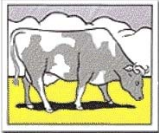
Uses for Simulation





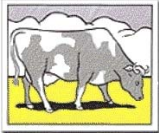
Causes of Inaccuracy

- Many possible causes
 - Software differences
 - Hardware differences
 - System effects
 - Time dilation: interaction with physical world
- Here, we consider:
 - Operating system code
 - DMA traffic
 - Wrong-path effects

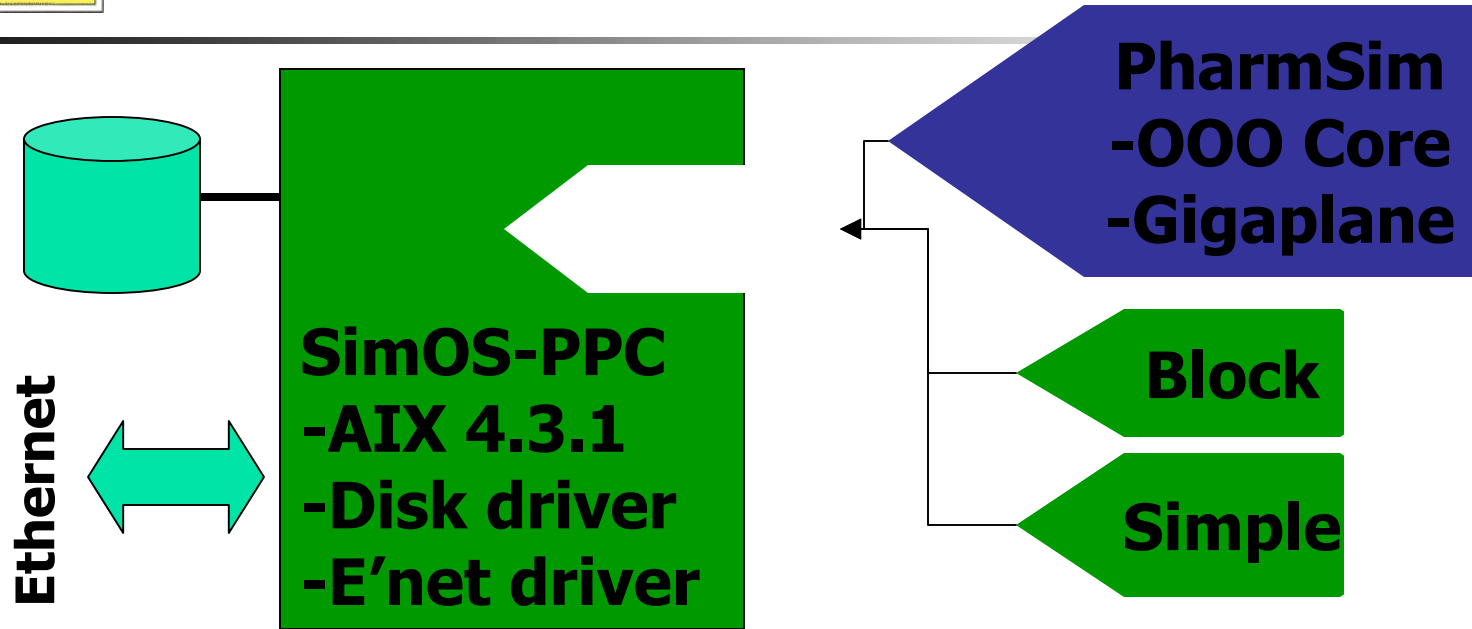


Validating Accuracy

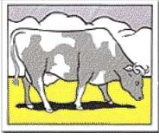
- How do we validate?
 - Against real hardware with perf. counters
 - Different "input" since O/S now present
 - Also, post-mortem: too late
 - Against HDL
 - Same *input* as model, same error?
- Without full system simulation, cannot:
 - Replicate runtime environment
 - Cannot really validate accuracy
- Compensating errors mask inaccuracy
- Hence: build simulator that does not cheat



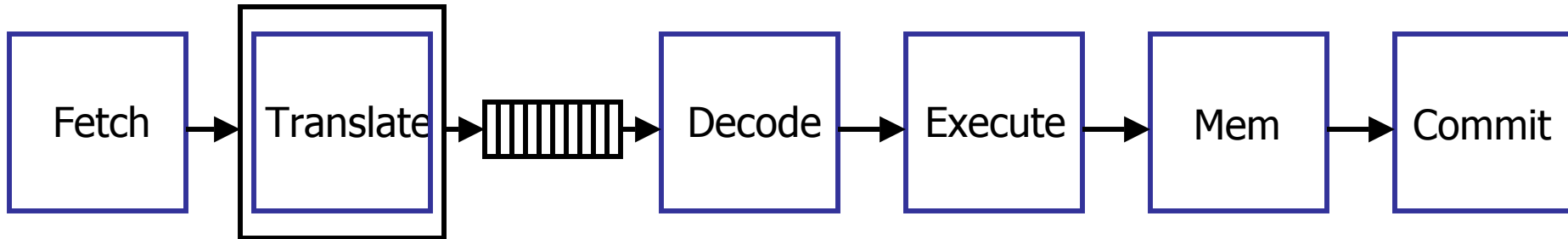
PharmSim Overview



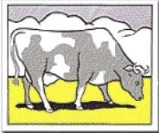
- Device simulation, etc. from SimOS-PPC
- PharmSim replaces functional simulators
 - Full OOO core model, values in rename registers
 - Based on SimpleMP [Rajwar]
 - Adds priv. mode, MMU, TLB, exceptions, interrupts, barriers, flushes, etc.



PharmSim Pipeline

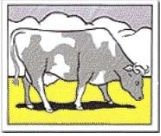


- Substantially similar to IBM Power4
 - Some instructions “cracked” (1:2 expansion)
 - Others (e.g. lmw) microcode stream
- Mem Stage
 - Interface to 2-level cache model
 - Sun Gigaplane XB snoopy MP coherence
 - Caches contain values, must remain coherent
- No cheating!
 - No “flat” memory model for reference/redirect



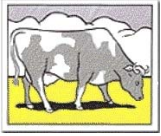
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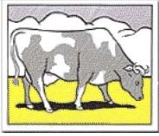
Operating System Effects

- Fairly well-understood for commercial:
 - Must account for O/S references
- For SPEC? Widely accepted:
 - Safe to ignore O/S paths
 - Most popular tool (SimpleScalar)
 - Intercepts system calls
 - Emulates on host, updates “flat” memory
 - Returns “magically” with caches intact
 - Is this really OK?

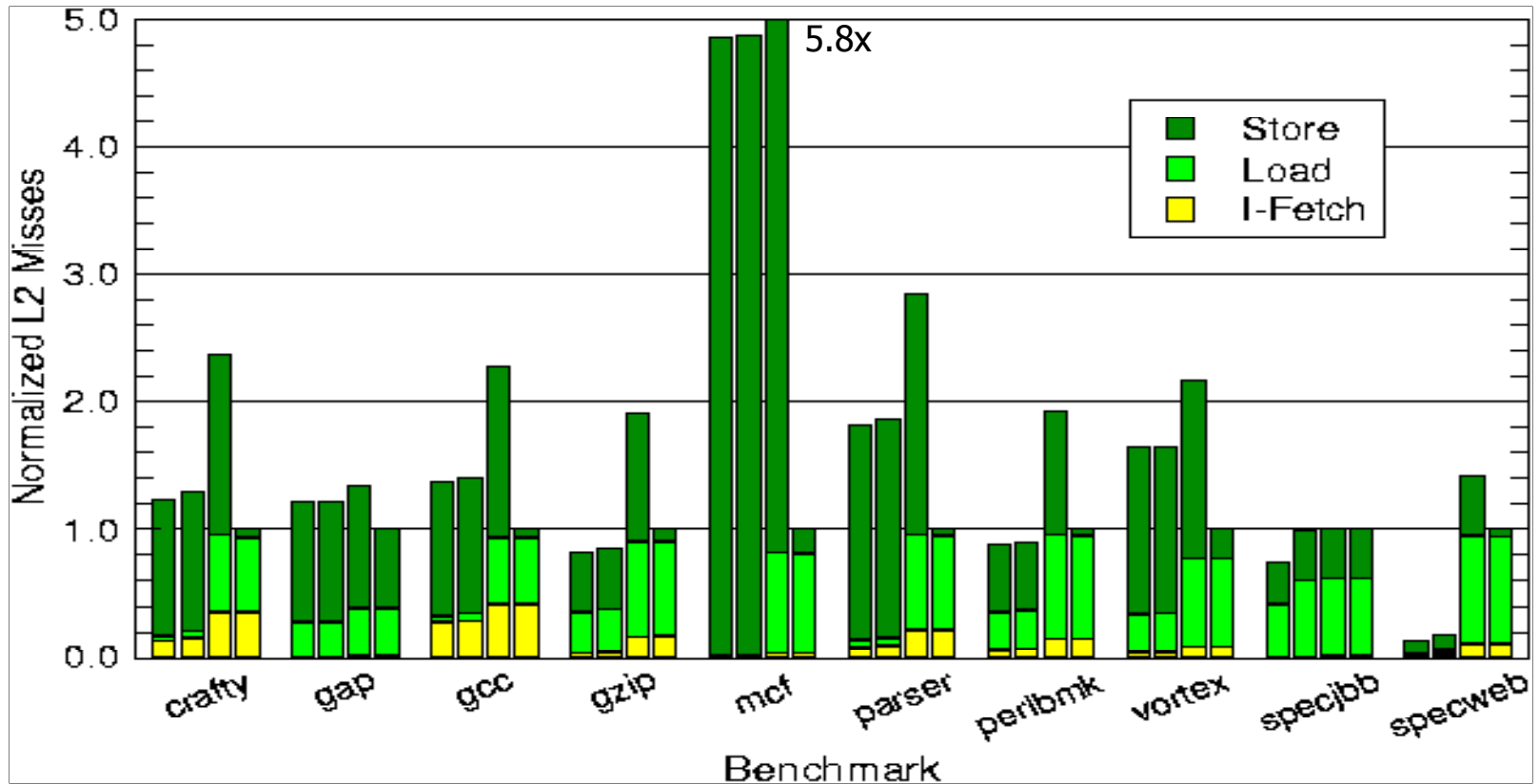


Operating System Effects

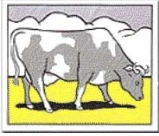
References Modeled	Example
User-mode only	Atom
User + Shared library	Simplescalar with static link
User + Sh Lib + O/S	H/W bus trace
User + Sh Lib + O/S + cache control ops	PharmSim



Operating System Effects

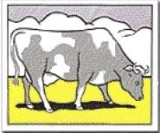


- Dramatic error (5.8x in mcf, 2-3x commonplace)
- Note compensating errors (e.g. *crafty*, *gzip*, *perl*)
- IPC error > 100% (more detail at ISCA)

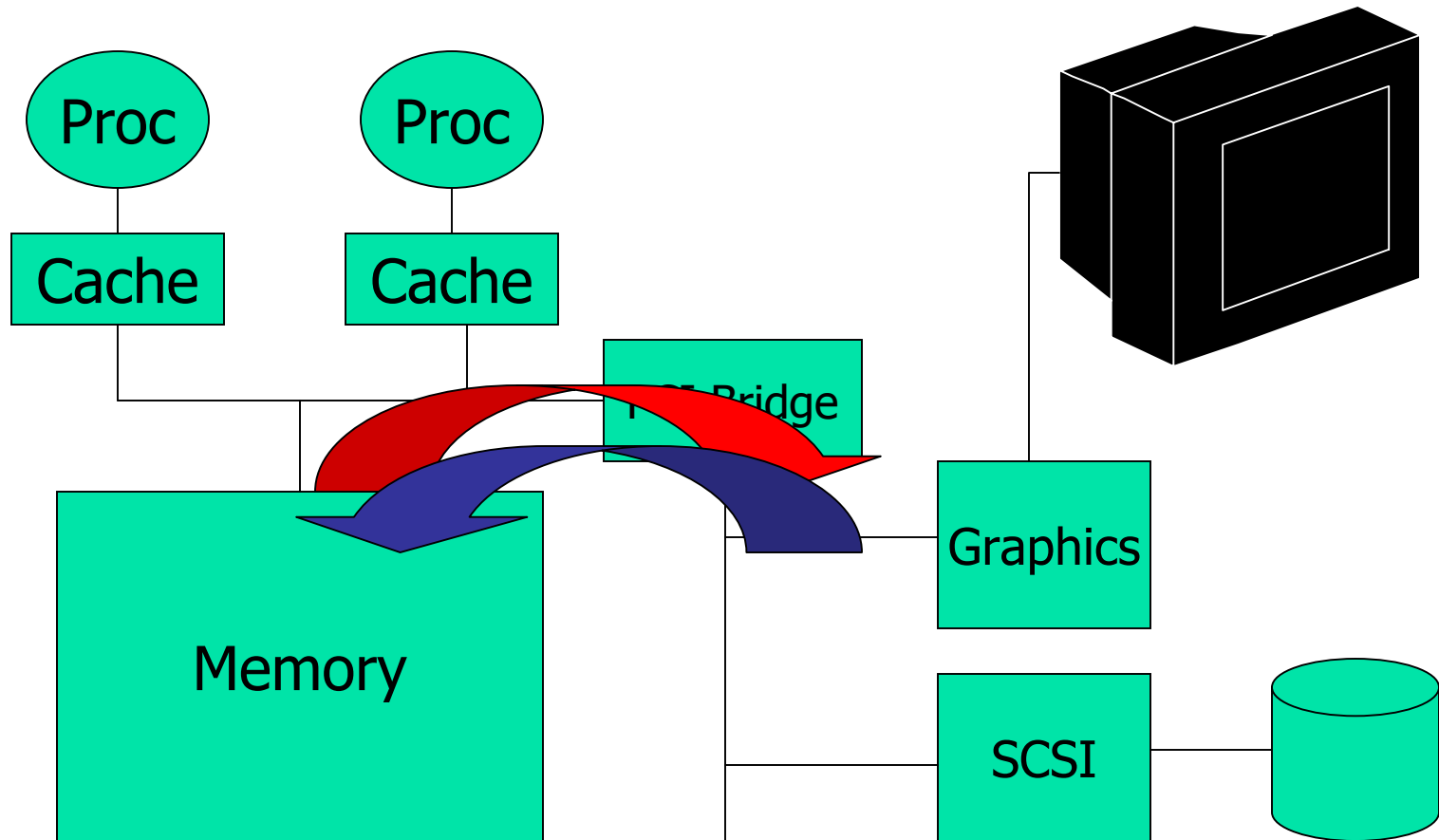


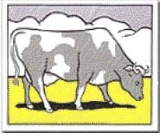
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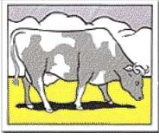
Coherent I/O with DMA





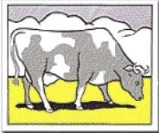
DMA Traffic

- How do we support DMA?
 - No “flat” memory image in simulator
 - Lines may be in caches
 - Invalidate (if DMA write)
 - Flush (if DMA read)
- Must use existing coherence protocol
 - Everything has to work correctly
 - No subtle coherence bugs
- How much does this matter?
 - Affects cache miss rates
 - Introduces bus contention



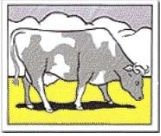
DMA Traffic

- PharmSim incorporates accurate DMA engine:
 - Issues bus invalidates, snoops
 - Concurrent data transfer: **No "magic" flat memory**
- Bottom line:
 - Unimportant for SPECINT
 - Unimportant for SPECWEB, SPECJBB
 - Others in progress
 - Contrived multiprogrammed workload
 - 4.8% of all coherence traffic due to I/O, 1% IPC effect
- Results understated due to "overbuilt" MP bus
 - MP workloads likely much more sensitive
 - Additional evaluation in progress

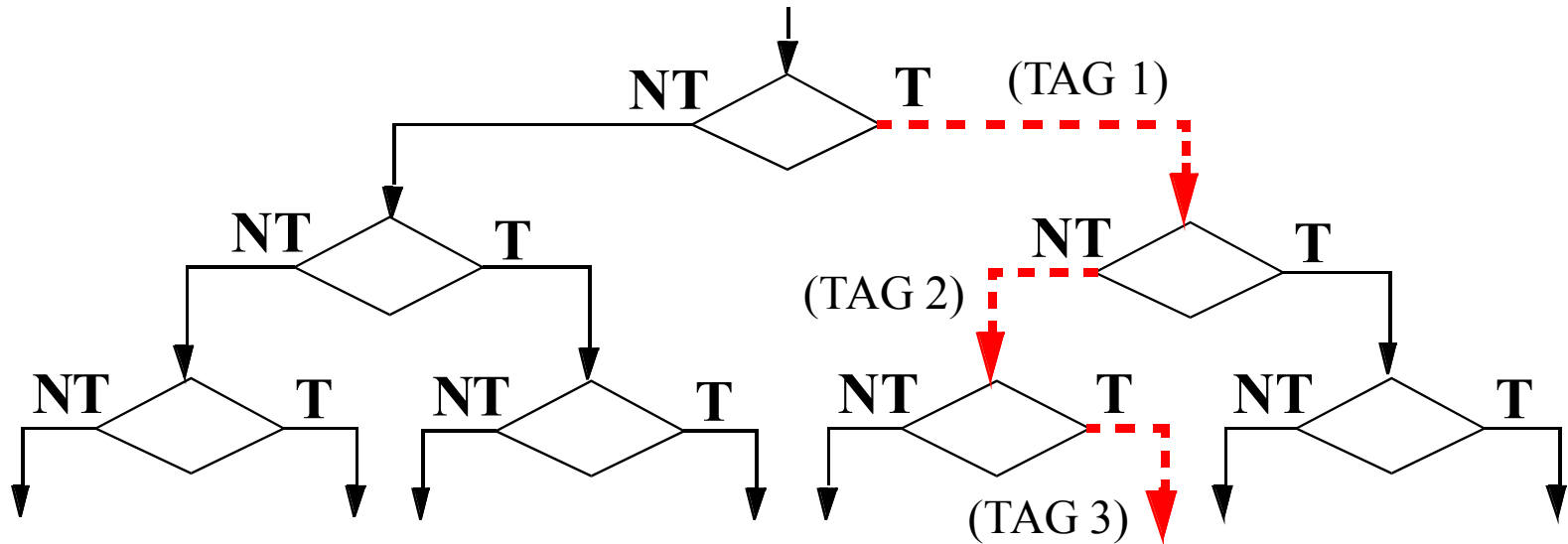


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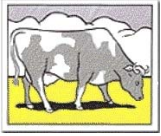
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Wrong-Path Execution

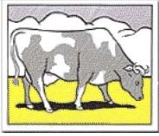


- Branch predictor predicts control flow
- Branch execute redirects mispredictions
- Extra instructions on wrong path

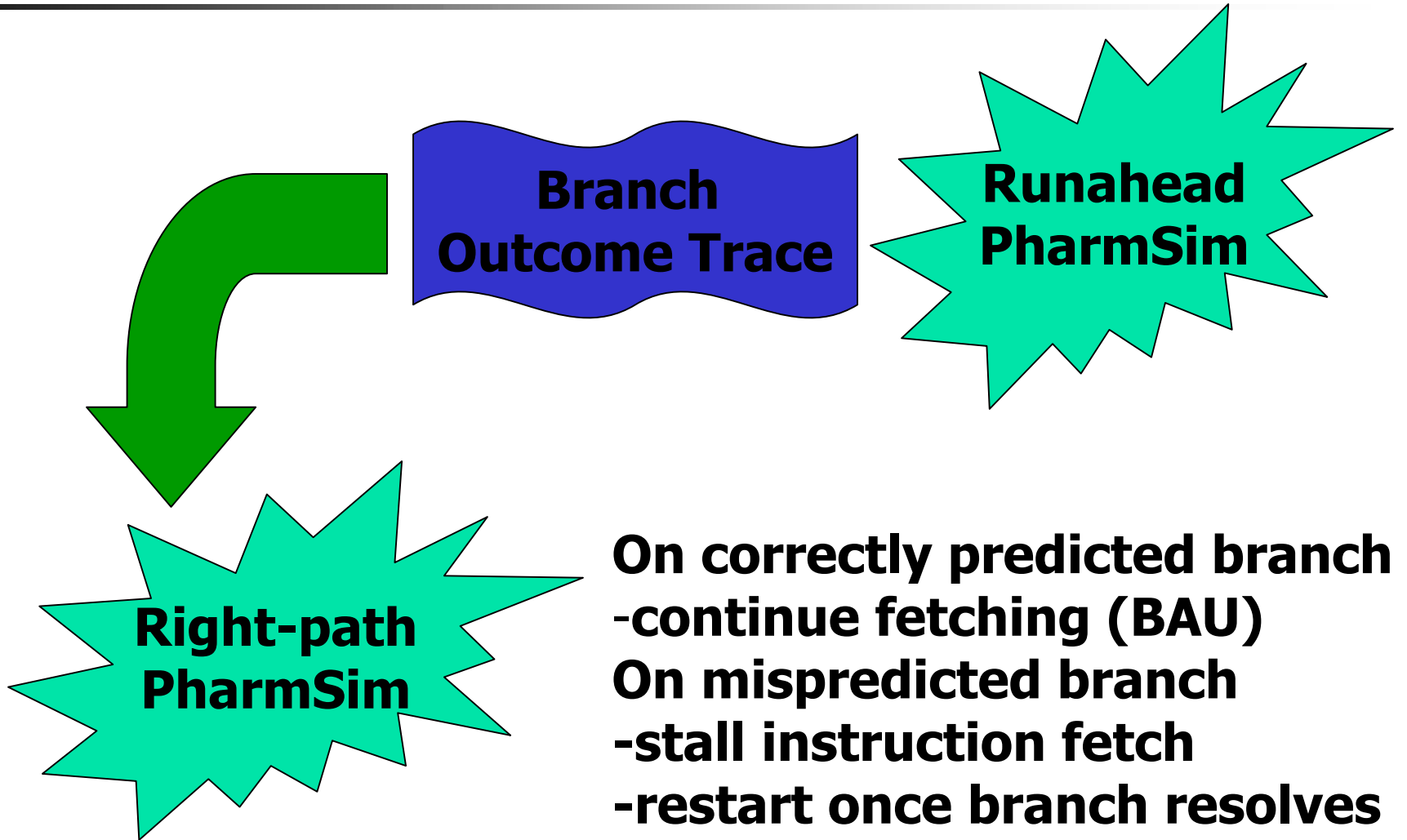


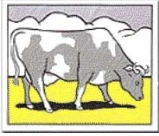
Wrong-path Execution

- Multiple effects on unarchitected state
 - Pollute/prefetch I-cache, D-cache, TLB
 - Pollute/train branch predictor (BHR, PHT, RAS)
- PharmSim (current status):
 - BHR is updated and repaired
 - PHT is not updated speculatively
 - RAS is updated, no repair
 - No speculative TLB fill
- How can we filter wrong-path instructions?
 - No “cheating”: don’t know branch outcomes

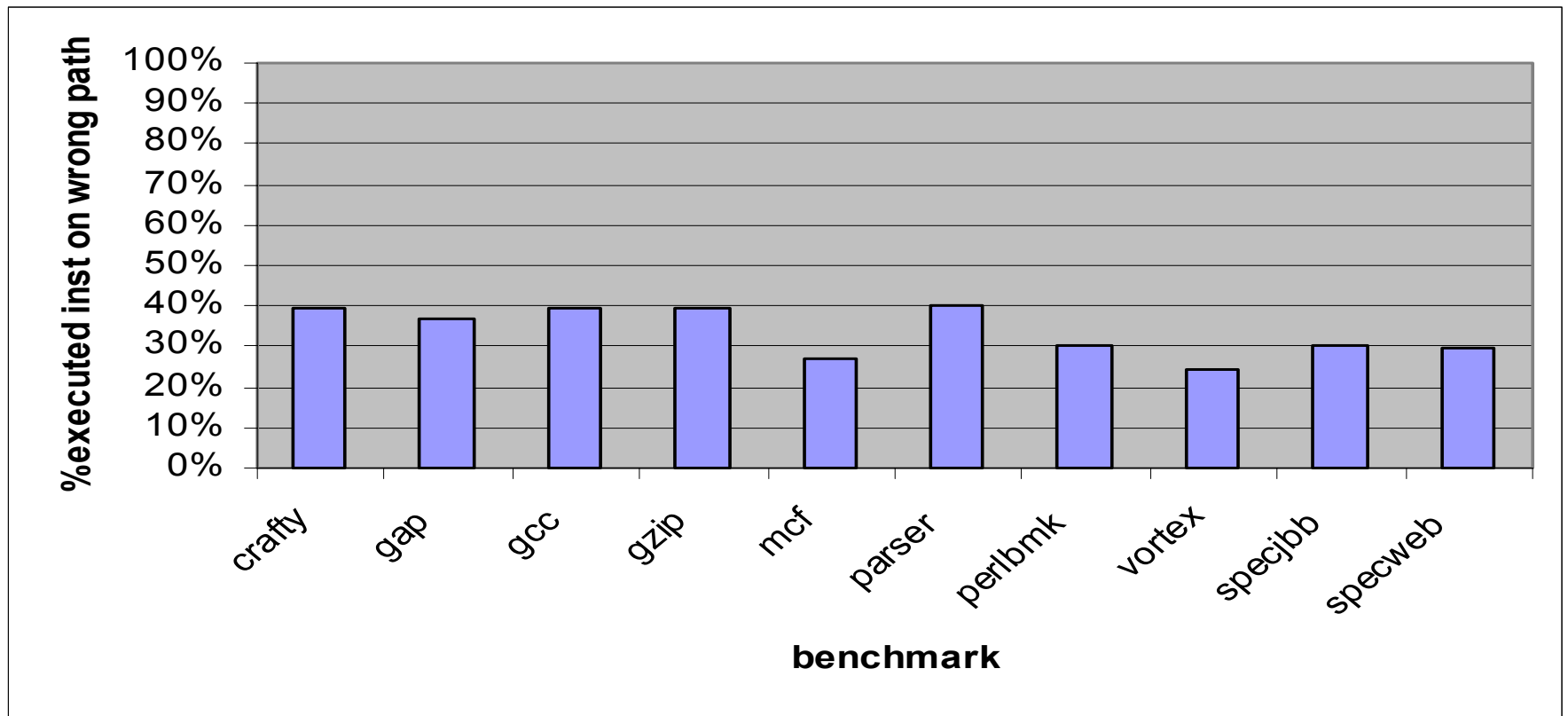


Eliminating Wrong-Path

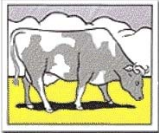




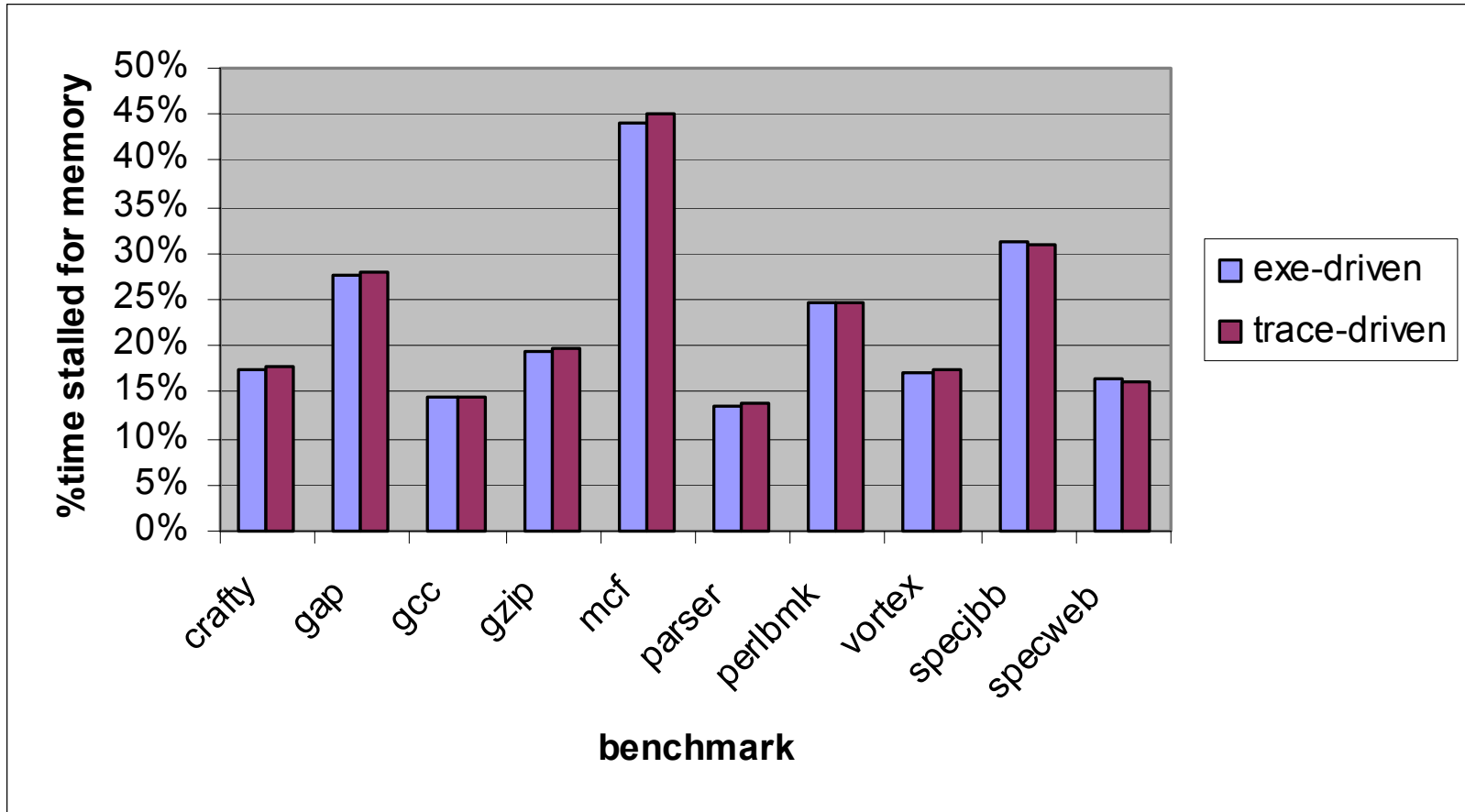
Wrong-path Instructions



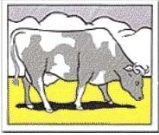
- Aggressive core model; 25%-40% wrong-path



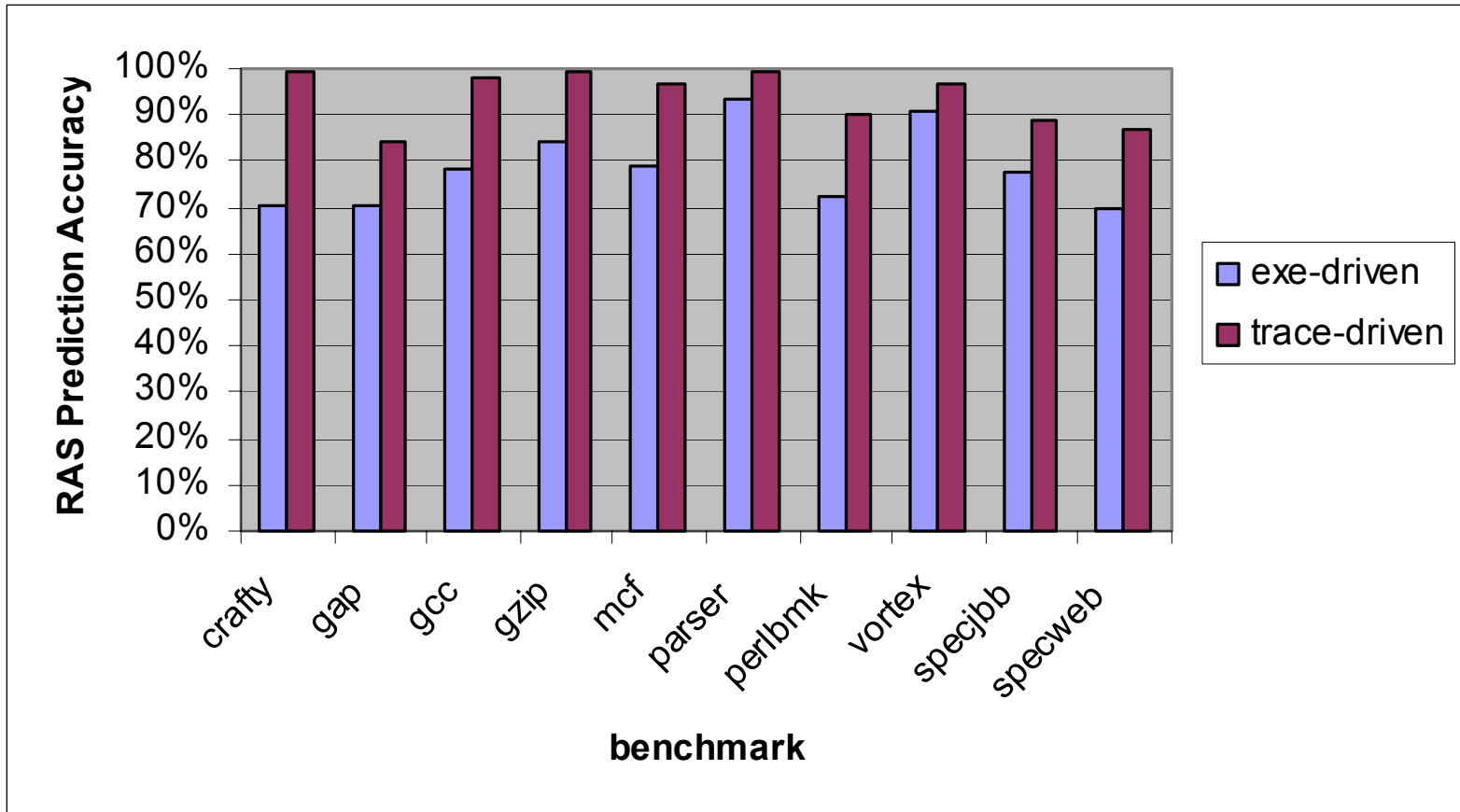
Wrong-path Memory Stalls



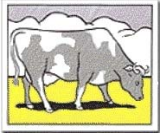
- Minor effect: better or worse



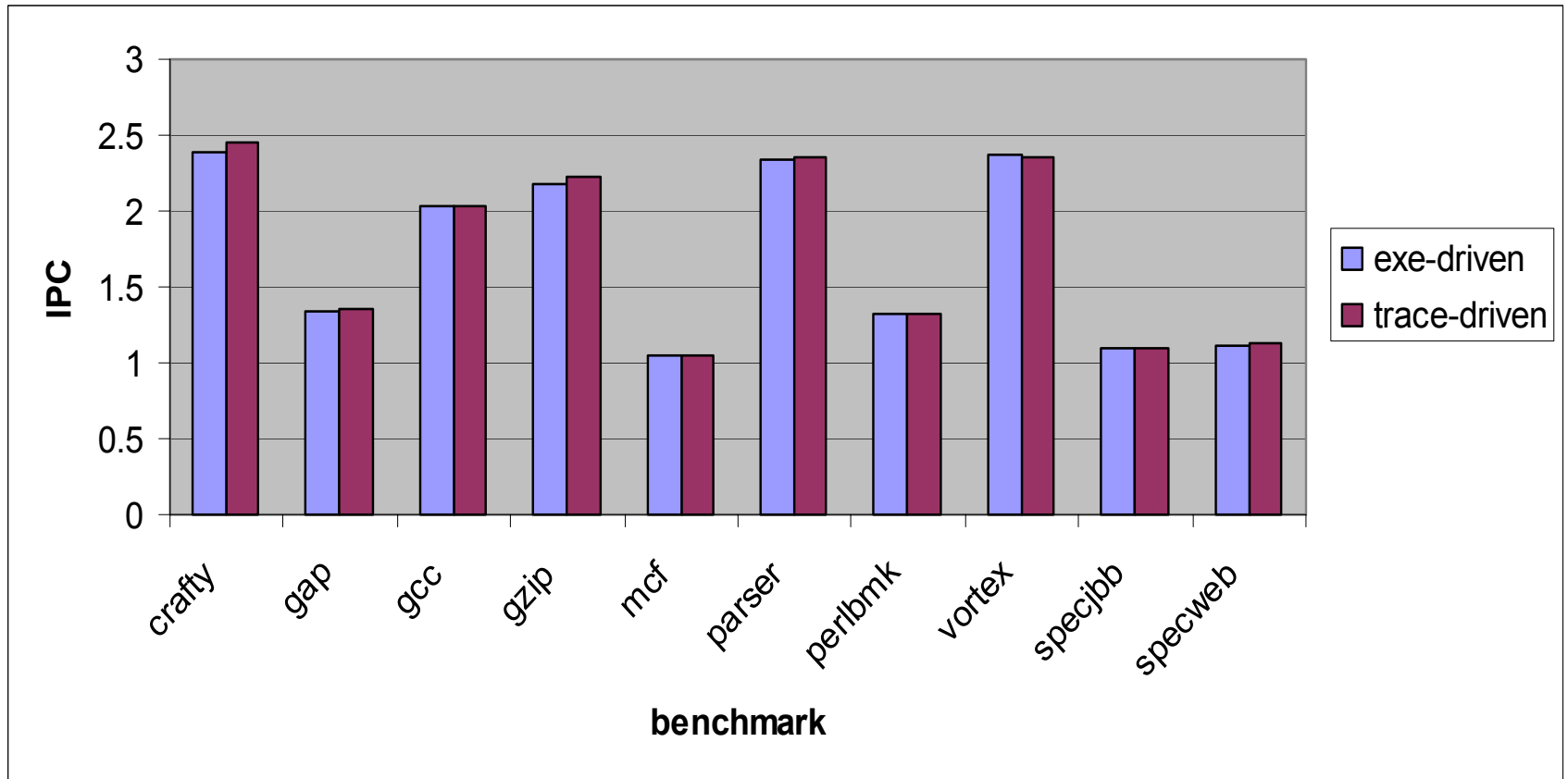
Wrong-path RAS Accuracy



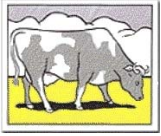
- Prediction accuracy degrades up to 29%
- Could add fixup logic



Wrong-path IPC

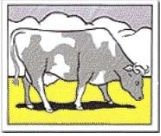


- Negligible effect (0.9%)
- RAS mispredictions overlapped



Summary

- PharmSim
 - Simulator that does not *cheat*
 - Can be used to validate assumptions, simplifications, abstractions
- Evaluated three effects on accuracy
 - O/S: dramatic error, even for SPECINT
 - DMA: not important for uniprocessors
 - MP, bus-constrained results TBD
 - Wrong path: unimportant



Conclusions

- Ignoring O/S effects fraught with danger
 - Should **always** model O/S effects
- Trace-driven vs. execution-driven
 - Traces with O/S much better
 - Invest in
 - **Trace quality** vs.
 - **Complexity** of execution-driven simulation
- Precision without accuracy?
 - Of questionable value
- Validation difficult due to compensating errors
 - Hard to know if model is precise or accurate