CURRICULUM VITAE

MIKKO H. LIPASTI

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RESEARCH INTERESTS AND IMPACT

Design, modeling, measurement, and analysis of neurally-inspired and conventional high-performance computing substrates, architectures, and algorithms.

Google Scholar: 4851 citations (1938 since 2010), h-index 36 (22 since 2010)

One of only 15 researchers worldwide in every Hall of Fame (ISCA, MICRO, HPCA)

EDUCATION

Ph.D. in Electrical and Computer Engineering, Carnegie Mellon University, May 1997
Advisor: John Paul Shen Thesis: Value Locality and Speculative Execution

M.S. in Electrical and Computer Engineering, Carnegie Mellon University, Dec. 1992
Advisor: John Paul Shen Thesis: Compilation Techniques for Superscalar Processors

B.S. in Computer Engineering, Valparaiso University, May 1991
Graduated summa cum laude

EMPLOYMENT HISTORY

2012-present — Co-founder. Thalchemy Corporation, Madison, WI
Co-founded Thalchemy Corp, a startup company that is developing novel algorithms and accelerators to enable ultra low-power continuous sensory processing in smartphones and other battery-operated devices. Thalchemy's algorithms are based on research conducted at UW-Madison over the last seven years, and effectively mimic the operation of the mammalian thalamus, which serves as the routing, filtering, and preprocessing point for all sensory data on its way to the neocortex. Thalchemy has secured multiple grants from NSF and other sources, and successfully closed a seed funding round with two institutional venture capital firms in June 2014.

2009-present — Professor. Department of ECE, University of Wisconsin, Madison, WI
Named to Philip Dunham Reed Endowed Professorship. Supervised nine additional Ph.D. theses to completion (total of 17 to date). Currently supervising seven graduate and two undergraduate researchers, with focus areas in cortical/neural information processing, high-performance processor microarchitecture, on-chip interconnects, and CMOS reliability.

2005-2009 — Associate Professor. Department of ECE, University of Wisconsin, Madison, WI
Supervised five additional Ph.D. theses to completion (total of eight). Led restructuring of introductory computer engineering curriculum, introduced a new freshman course which is attracting many new students to the field, and developed new course in mobile systems programming. Post-tenure research directions include CMOS chip power and reliability, electrical and optical on-chip interconnection networks, dynamic code optimization, and cortical/neural information processing.

2004-2006 — Microarchitectural Consultant. Intel Corporation, Austin, TX
Participated in research and development of future microprocessor microarchitecture and system architecture.

1999-2005 — Assistant Professor. Department of ECE, University of Wisconsin, Madison, WI

Created a substantial and very successful research program at University of Wisconsin, which is (informally) the top-ranked computer architecture research university in the world, raising over $4M in funding and equipment over 6-year probationary period. Supervised 3 Ph.D. theses and 14 M.S. projects to completion.

1997-1999 Advisory Engineer/Scientist. IBM Corporation, Rochester, MN
I participated in microarchitectural definition and predictive performance analysis of future AS/400 and RS/6000 processors and systems. This encompassed processor core and memory subsystem timer model implementation, design trade-off analysis, and creative problem-solving requiring original invention resulting in several patent applications.

1998-1999 Adjunct Faculty. University of Minnesota, Minneapolis, MN
I taught an advanced graduate-level class on computer architecture offered through the Department of Electrical and Computer Engineering (ECE) to a combined enrollment of 40 students. Class research projects resulted in two conference paper submissions.

1995-1997 Research Assistant. Carnegie Mellon University, Pittsburgh, PA
I conducted original research in memory subsystems, value prediction, and superspeculative processor microarchitecture; performed a detailed evaluation of the PowerPC 620; implemented accurate microarchitectural timing models; and implemented trace-driven and emulation-based tools for modeling and characterizing processor performance.

1993-1995 Performance Analyst/Programmer. IBM Corporation, Rochester, MN
I was involved in predictive performance analysis of future AS/400 processors, operating systems, and compilers; modeling and visualization of memory subsystem behavior; and implementation of operating system kernel functions, while initiating or making significant contributions to the filing of four U.S. patent applications.

1991-1993 Research/Teaching Assistant. Carnegie Mellon University, Pittsburgh, PA
I conducted original research in instruction scheduling, register allocation, and computer architecture; designed and implemented a binary-to-binary recompilation system for the IBM RS/6000 that performs global, trace-based scheduling and register renaming; and assisted in teaching senior- and sophomore-level computer engineering courses.

1990 Co-op Engineer. Process Automation, Inland Steel Co., East Chicago, IN
I maintained and enhanced real-time process control and data collection software.

HONORS AND ACHIEVEMENTS

Hilldale Undergraduate/Faculty Research Fellowship, 2015, advisee: Erik Jorgensen

HPCA Hall of Fame, 2015 (inaugural member)

Co-founded Thalchemy Corp. to commercialize research in neurally-inspired computing

IEEE Fellow, 2013

HPCA 2014 Best Paper Nominee (top 3% of 215 submissions)

IISWC 2012 Best Paper Nominee

IPDPS 2011 Best Paper in Track

MICRO Hall of Fame, 2009 (inaugural member)

ISCA Hall of Fame, 2008 (inaugural member)

Awarded Philip Dunham Reed Endowed Chair, 2008-present

Outstanding Young Alumnus Award, Valparaiso University, 2007

Gerald Holdridge Teaching Excellence Award, 2006

IEEE MICRO “Top Picks” papers: 2004, 2006

ISPASS 2004 Best Paper Award

Eta Kappa Nu Outstanding Young Electrical Engineer, 2002

Peter Schneider Computer Engineering Junior Faculty Fellowship, 2002

Hilldale Undergraduate/Faculty Research Fellowship, 2002, advisee: Erika Gunadi

NSF CAREER Award, 2001

Eta Kappa Nu Outstanding Young Electrical Engineer Honorable Mention, 1999

IBM Server Group Patent Issuance Award, 1997

Best Paper Award, MICRO-29, Paris, December 1996.

IBM First Plateau Invention Achievement Award, March 1996

IBM Technical Recognition Award, July 1995

Tau Beta Pi National Engineering Honor Society

Completed undergraduate curriculum in six semesters

BOOKS AND BOOK CHAPTERS

1. John Paul Shen and Mikko H. Lipasti, "*Modern Processor Design: Fundamentals of Superscalar Processors*," Paperback Edition, Waveland Press, 2013.
2. John Paul Shen and Mikko H. Lipasti, "*Modern Processor Design: Fundamentals of Superscalar Processors*," First Edition, McGraw-Hill Companies, 2005. Adopted by 29+ universities.
3. John Paul Shen and Mikko H. Lipasti, "*Modern Processor Design: Fundamentals of Superscalar Processors*," Beta Edition, McGraw-Hill Companies, 2003.
4. Craig Saldanha and Mikko H. Lipasti, "Power Efficient Cache Coherence," in *High-Performance Memory Systems*, edited by H. Hadimiouglu, D. Kaeli, J. Kuskin, A. Nanda, and J. Torrellas, Springer-Verlag, 2003.
5. Jason Cantin, Mikko H. Lipasti, and James E. Smith, "Dynamic Verification of Cache Coherence Protocols," in *High-Performance Memory Systems*, edited by H. Hadimiouglu, D. Kaeli, J. Kuskin, A. Nanda, and J. Torrellas, Springer-Verlag, 2003.

JOURNAL PUBLICATIONS

6. Zhong Zheng, Z. Wang, and Mikko Lipasti, "Adaptive Cache and Concurrency Allocation on GPGPUs," *IEEE Computer Architecture Letters*, vol. PP, issue 99, 2014.
7. David J. Palframan, Nam Sung Kim, and Mikko H. Lipasti, "Resilient High-Performance Processors with Spare RIBs," *IEEE MICRO* (special issue on reliability), 2013.
8. Andrew Nere, Sean Franey, Atif Hashmi, and Mikko Lipasti, "Simulating Cortical Networks on Heterogeneous Multi-GPU Systems,"*Journal of Parallel and Distributed Computing*, http://dx.doi.org/10.1016/j.jpdc.2012.02.006, 73(7), pages 953–971, 2012.
9. Atif Hashmi and Mikko Lipasti, "A Cortically Inspired Learning Model," *Studies in Computational Intelligence*, Vol. 399, 2012.
10. Natalie Enright Jerger and Mikko Lipasti, "Systems for Very Large-Scale Computing," *IEEE MICRO Special Issue* (guest editors' introduction), Vol. 31, No. 3, pp. 4-7, 2011.
11. Natalie Enright Jerger, Mikko Lipasti, and Li-Shiuan Peh, "Circuit-switched Coherence," *IEEE Computer Architecture Letters*, Vol. 6, No. 1, Jan-Jun, 2007.
12. Erika Gunadi and Mikko H. Lipasti, "Narrow Width Dynamic Scheduling," *Journal of Instruction-level Parallelism*, Vol. 9, No. 1, April 2007.
13. Eric F. Weglarz, Kewal K. Saluja, and Mikko H. Lipasti, "Energy Estimation of the Memory Subsystem in Multiprocessor Systems," *Journal of Low-Power Electronics*, Vol. 2, No. 3, December 2006, pp. 325-332.

14. Jason Cantin, Mikko H. Lipasti, James E. Smith, Andreas Moshovos, and Babak Falsafi, ”Coarse-Grain Coherence Tracking: RegionScout and Region Coherence Arrays,” *IEEE MICRO Special Issue on Top Picks in Computer Architecture*, Vol. 26, No. 1, pp. 70-79, 2006.
15. Jason Cantin, Mikko H. Lipasti, and James E. Smith, "The Complexity of Verifying Memory Coherence and Consistency," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 16, No. 7, July 2005.
16. Harold Cain and Mikko H. Lipasti, "Memory Ordering: A Value-based Approach," *IEEE MICRO Special Issue on Top Picks in Computer Architecture*, vol. 24, no. 6, pp. 110-117, 2004.
17. Harold W. Cain, Mikko H. Lipasti, and Ravi Nair “Constraint Graph Analysis of Multithreaded Programs,” *Journal of Instruction-level Processing (JILP)*, Vol. 6, 2004.
18. Kevin Lepak, Gordon Bell, and Mikko Lipasti, “Silent Stores and Store Value Locality,” *IEEE Transactions on Computers*, pp. 1174-1190, Vol. 50, No. 11, November 2001.
19. S.R. Kunkel, R.J. Eickemeyer, M.H. Lipasti, T.J. Mullins, B. O’Krafka, H. Rosenberg, S.P. VanderWiel, P.L. Vitale, and L.D. Whitley, “A Performance Methodology for Commercial Servers,” *IBM Journal of Research and Development*, Vol. 44, No. 6, 2000.
20. Mikko H. Lipasti and John Paul Shen, “Exploiting Value Locality to Exceed the Dataflow Limit,” *International Journal of Parallel Processing*, Vol. 26, No. 4, pp. 505-538, 1998.
21. Mikko H. Lipasti and John Paul Shen, “A Superspeculative Microarchitecture for A.D. 2000 and Beyond,” *IEEE Computer Special Issue: Future Microprocessors--How to use a Billion Transistors*, September 1997.

REFEREED CONFERENCE PUBLICATIONS

22. Rohit Shukla and Mikko H. Lipasti, “A Self-Organizing Map-Seeking Circuit For Visual Object Recognition,” in *Proceedings of the 2015 International Joint Conference on Neural Networks (IJCNN 2015)*, Killarney, Ireland, July 2015
23. David J. Palframan, Nam Sung Kim, and Mikko H. Lipasti, “COP: To Compress and Protect Main Memory,” in *Proceedings of the 42nd International Symposium on Computer Architecture (ISCA-42)*, Portland, OR, June 2015.
24. Amir Yazdanbakhsh, David Palframan, Azadeh Davoodi, Nam Sung Kim and Mikko Lipasti , “Online and Operand-Aware Detection of Failures Utilizing False Alarm Vectors,” in *Proceedings of the 2015 Great Lakes Symposium on VLSI (GLSVLSI-2015)*, Pittsburgh, PA, May 2015.
25. David J. Palframan, Nam Sung Kim, and Mikko H. Lipasti , “iPatch: Intelligent Fault Patching to Improve Energy Efficiency,” in *Proceedings of the 21st IEEE International Symposium on High Performance Computer Architecture (HPCA 2015)*, San Francisco, CA, Feb. 2015.
26. Sean Franey and Mikko H. Lipasti, “Tag Tables,” in *Proceedings of the 21st IEEE International Symposium on High Performance Computer Architecture (HPCA 2015)*, San Francisco, CA, Feb. 2015.
27. Dibakar Gope and Mikko Lipasti, “Bias-Free Branch Prediction,” in *Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-47)*, Cambridge, UK, Dec. 2014.
28. Zhong Zheng and Mikko H. Lipasti, “Tag Check Elision,” in *Proceedings of the IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED),* La Jolla, CA, August 2014.

29. Dibakar Gope and Mikko H. Lipasti, "Atomic SC for Simple In-order Processors," in *Proceedings of the 20th IEEE International Symposium on High Performance Computer Architecture (HPCA 2014)*, Orlando, FL, Feb. 2014. (**nominated for best paper award**)
30. Mitchell Hayenga, Vignyan Reddy, and Mikko H. Lipasti , "Revolver: Processor Architecture for Power Efficient Loop Execution," in *Proceedings of the 20th IEEE International Symposium on High Performance Computer Architecture (HPCA 2014)*, Orlando, FL, Feb. 2014.
31. David J. Palframan, Nam Sung Kim, and Mikko H. Lipasti, "Precision-Aware Soft Error Protection for GPUs," in *Proceedings of the 20th IEEE International Symposium on High Performance Computer Architecture (HPCA 2014)*, Orlando, FL, Feb. 2014.
32. Arslan Zulfiqar, Pranay Koka, Herb Schwetman, Mikko Lipasti, Xuezhe Zheng, and Ashok V. Krishnamoorthy, "Wavelength Stealing: An Opportunistic Approach to Channel Sharing in Multi-chip Photonic Interconnects," in *Proceedings of the 46th Annual IEEE/ ACM International Symposium on Microarchitecture (MICRO-46)), Davis, CA, Dec. 2013.*
33. Mushfique Khurshid and Mikko Lipasti, "Data Compression for Thermal Mitigation in the Hybrid Memory Cube," in *Proceedings of the 31st IEEE International Conference on Computer Design (ICCD 2013)*, Asheville, NC, Oct. 2013.
34. Vignyan Kothinti Naresh, Syed Gilani, Michael Schulte, Nam Sung Kim, and Mikko Lipasti, "REEL: Reducing Effective Execution Latency of Floating Point Operations," in *Proceedings of the IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Beijing, China, Sep. 2013.
35. Sean Franey and Mikko Lipasti, "Accelerating Atomic Operations on the GPU for Broader Applicability," in *Proceedings of the 7th International Symposium on Networks-on-Chip (NOCS 2013)*, Tempe, AZ, April 2013.
36. Andrew Nere, Atif Hashmi, Mikko Lipasti, and Giulio Tononi, "Bridging the Semantic Gap: Emulating Biological Neuronal Behaviors with Simple Digital Neurons," in *Proceedings of the 19th IEEE International Symposium on High-Performance Computer Architecture (HPCA-19)*, Shenzhen, China, February 2013.
37. Tianshi Chen, Yunji Chen, Marc Duranton, Qi Guo, Atif Hashmi, Mikko Lipasti, Andrew Nere, Shi Qiu, Michele Sebag, and Olivier Temam, BenchNN: On the Broad Potential Application Scope of Hardware Neural Network Accelerators," in *Proceedings of the 2012 IEEE International Symposium on Workload Characterization (IISWC 2012)*, San Diego, CA, Nov. 2012 (**nominated for best paper award**).
38. David Palframan, Nam Sung Kim, and Mikko H. Lipasti, "Mitigating Random Variation with Spare RIBs: Redundant Intermediate Bitslices," in *Proceedings of the 42nd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2012)*, Boston, MA, June 2012.
39. Mitch Hayenga and Mikko H. Lipasti, "The NoX Router," in *Proceedings of the 44th Int'l Symposium on Microarchitecture (MICRO-44)*, Porto Alegre, Brazil, December 2011.
40. Vignyan Kothinti Naresh, David Palframan, and Mikko H. Lipasti, "CRAM: Coded Registers for Amplified Multiporting," in *Proceedings of the 44th Int'l Symposium on Microarchitecture (MICRO-44)*, Porto Alegre, Brazil, December 2011.
41. Atif Hashmi, Hugues Berry, Olivier Temam, and Mikko H. Lipasti, "Automatic Abstraction and Fault Tolerance in Cortical Microarchitectures," in *Proceedings of the 38th International Symposium on Computer Architecture (ISCA-38)*, San Jose, CA, June 2011.
42. Erika Gunadi and Mikko H. Lipasti, " CRIB: Combined Rename, Issue, and Bypass," in *Proceedings of the 38th International Symposium on Computer Architecture (ISCA-38)*, San Jose, CA, June 2011.

43. Andrew Nere, Atif Hashmi, and Mikko H. Lipasti, "Profiling Heterogeneous Multi-GPU Systems to Accelerate Cortically Inspired Learning Algorithms," in *Proceedings of the 25th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2011)*, Anchorage, Alaska, May 2011.
44. Guangyu Shi, Min Li, and Mikko H. Lipasti, "Accelerating Search and Recognition Workloads with SSE 4.2 String and Text Processing Instructions," in *Proceedings of the 2011 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2011)*, Austin, TX, April 2011.
45. David J. Palframan, Nam Sung Kim, and Mikko H. Lipasti, "Time Redundant Parity for Low-Cost Transient Error Detection," in *Proceedings of Design, Automation, and Test in Europe (DATE 2011)*, Grenoble, France, March 2011.
46. Atif Hashmi, Andrew Nere, James Thomas, and Mikko Lipasti, "A Case for Neuromorphic Instruction Set Architectures," in *Proceedings of the 16th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2011)*, Newport Beach, CA, March 2011.
47. Dana Vantrease, Nate Binkert, and Mikko H. Lipasti, "Atomic Coherence: Leveraging Nanophotonics to Build Race-Free Cache Coherence Protocols," in *Proceedings of the 17th IEEE International Symposium on High-Performance Computer Architecture (HPCA-17)*, San Antonio, TX, February 2010.
48. Erika Gunadi, Abhisek A. Sinkar, Nam Sung Kim, and Mikko Lipasti, "Combating Aging with the Colt Duty Cycle Equalizer," in *Proceedings of the 43rd Int'l Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, December 2010.
49. Atif Hashmi and Mikko Lipasti, "Discovering Cortical Algorithms," in *Proceedings of the International Conference on Neural Computation (ICNC)*, Valencia, Spain, October 2010.
50. Mitchell Hayenga, Natalie D. Enright Jerger, and Mikko H. Lipasti, "SCARAB: A Single Cycle Adaptive Routing and Bufferless Network," in *Proceedings of the 42nd Int'l Symposium on Microarchitecture (MICRO-42)*, New York, NY, December 2009.
51. Dana Vantrease, Nate Binkert, Robert Schreiber, and Mikko H. Lipasti, " Light speed arbitration and flow control for nanophotonic interconnects," in *Proceedings of the 42nd Int'l Symposium on Microarchitecture (MICRO-42)*, New York, NY, December 2009.
52. Dennis Abts, Natalie D. Enright Jerger, John Kim, Dan Gibson, and Mikko Lipasti, "Achieving Predictable Performance Through Better Memory Controller Placement in Many-Core CMPs,"in *Proceedings of the International Symposium on Computer Architecture (ISCA-36)*, Austin, TX, June 2009.
53. Atif Hashmi and Mikko H. Lipasti, "Cortical Columns: Building Blocks for Intelligent Systems," in *Proceedings of IEEE Symposium on Computational Intelligence for Multimedia Signal and Vision Processing (CIMSVP)*, Nashville, TN, March 2009.
54. Natalie Enright-Jerger, Li-Shiuan Peh and Mikko H. Lipasti, "Virtual Tree Coherence: Leveraging Regions In-Network Multicast Trees for Scalable Cache Coherence,"in *Proceedings of the 41st International Symposium on Microarchitecture (MICRO-41),* Italy, November 2008.
55. Gordon B. Bell and Mikko H. Lipasti, "Skewed Redundancy," in *Proceedings of the 17th International ACM/IEEE Conference on Parallel Architectures and Compilation Techniques (PACT-2008*), Toronto, Canada, October 2008.
56. Atif Hashmi and Mikko H. Lipasti, "Accelerating Search and Recognition with a TCAM Functional Unit," in *Proceedings of the 26th IEEE International Conference on Computer Design (ICCD-26)*, Lake Tahoe, CA, October 2008.
57. Eric L. Hill, Mikko H. Lipasti, and Kewal Saluja, "An Accurate Flip-flop Selection Technique for Reducing Logic SER," in *Proceedings of The 38th Annual IEEE/IFIP Interna-*

tional Conference on Dependable Systems and Networks (DSN-2008), Anchorage, Alaska, June 2008.

58. Natalie Enright-Jerger, Li-Shiuan Peh and Mikko H. Lipasti, "Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware Multicast Support," in *Proceedings of the 35th International Symposium on Computer Architecture (ISCA)*, Beijing, China, June 2008.
59. Natalie Enright Jerger, Li-Shiuan Peh, and Mikko H. Lipasti, "Circuit-switched Coherence," in *Proceedings of the IEEE Network on Chip Symposium (NOCS)*, Newcastle-Upon-Tyne, UK, April 2008.
60. Nidhi Aggarwal, Jason Cantin, Mikko H. Lipasti, and James E. Smith, "Power-Efficient DRAM Speculation," in *Proceedings of 14th International Symposium on High-Performance Computer Architecture (HPCA-14)*, Salt Lake City, UT, February 2008.
61. Erika Gunadi and Mikko H. Lipasti, "A Position-Insensitive Finished Store Buffer," in *Proceedings of the 25th IEEE International Conference on Computer Design (ICCD-25)*, Lake Tahoe, CA, October 2007.
62. Eric Hill and Mikko H. Lipasti, "Transparent Mode Flip-Flops for Collapsible Pipelines," in *Proceedings of the 25th IEEE International Conference on Computer Design (ICCD-25)*, Lake Tahoe, CA, October 2007 (short paper).
63. Natalie Enright Jerger, Dana Vantrease, and Mikko H. Lipasti, ""An Evaluation of Server Consolidation Workloads for Multi-core Designs," in *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*, Boston, MA, September 2007.
64. Erika Gunadi and Mikko H. Lipasti, "Power-Aware Operand Delivery," In *Proceedings of the IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)* , Portland, OR, August 2007 (short paper with poster presentation).
65. Lixin Su and Mikko H. Lipasti, "Speculative Optimization Using Hardware-Monitored Guarded Regions for Java Virtual Machines," In *Proceedings of of the 3rd International ACM Conference on Virtual Execution Environments (VEE-3)*, San Diego, CA, June 2007.
66. Jason F. Cantin, Mikko H. Lipasti, and James E. Smith, "Stealth Prefetching," in *Proceedings of the 12th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XII)*, October, 2006.
67. Eric L. Hill and Mikko H. Lipasti, Stall Cycle Redistribution in a Transparent Fetch Pipeline," in *Proceedings of the IEEE/ACM International Symposium on Low-Power Electronics and Design (ISLPED) 2006*, October, 2006.
68. Lixin Su and Mikko H. Lipasti, "Dynamic Class Hierarchy Mutation," in *Proceedings of of the 4th IEEE/ACM International Symposium on Code Generation and Optimization (CGO-4)*, New York, NY, March 2006.
69. Natalie Enright Jerger, Eric L Hill, and Mikko H. Lipasti, "Friendly Fire: Understanding the Effects of Multiprocessor Prefetching," in *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2006)*, Austin, TX, March 2006.
70. Shiliang Hu, Ilhyun Kim, Mikko H. Lipasti, and James E. Smith, "An Approach for Implementing Efficient Superscalar CISC Processors," In *Proceedings of of the 12th International Symposium on High-Performance Computer Architecture (HPCA-12)*, Austin, TX, February 2006.
71. J. F. Cantin, M. H. Lipasti, and J. E. Smith, "Improving Multiprocessor Performance with Coarse-Grain Coherence Tracking", in *Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32)*, Madison, WI, June 2005.
72. Kevin M. Lepak and Mikko H. Lipasti, "Reaping the Benefit of Temporal Silence to Improve Communication Performance," in *Proceedings of the IEEE International Sympo-*

sium on Performance Analysis of Systems and Software (ISPASS-2005), Austin, TX, March 2005.

73. Harold W. Cain and Mikko H. Lipasti, "Memory Ordering: A Value-Based Approach," in *Proceedings of the 31st International Symposium on Computer Architecture (ISCA-31)*, Munich, Germany, June 2004.
74. Mikko H. Lipasti, Brian Mestan, and Erika Gunadi, "Physical Register Inlining," in *Proceedings of the 31st International Symposium on Computer Architecture (ISCA-31)*, Munich, Germany, June 2004.
75. Gordon B. Bell and Mikko Lipasti, "Deconstructing Commit ," in *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2004)*, Austin, TX, March 2004 (Best Paper Award).
76. Ilhyun Kim and Mikko Lipasti, "Understanding Scheduling Replay Schemes ," in *Proceedings of the 10th International Symposium on High-Performance Computer Architecture (HPCA-10)*, Madrid, Spain, February 2004.
77. Ilhyun Kim and Mikko Lipasti, "Macro-op Scheduling: Relaxing Scheduling Loop Constraints ," in *Proceedings of the 36th International Symposium on Microarchitecture (MICRO-36)*, San Diego, CA, December 2003.
78. Kevin M. Lepak, Harold W. Cain, and Mikko H. Lipasti , "Redeeming IPC as a Performance Metric for Multithreaded Programs," in *Proceedings of the 12th International ACM/IEEE Conference on Parallel Architectures and Compilation Techniques (PACT-2003*), New Orleans, LA, September 2003.
79. Harold W. Cain, Mikko H. Lipasti, and Ravi Nair, "Constraint Graph Analysis of Multithreaded Programs," in *Proceedings of the 12th International ACM/IEEE Conference on Parallel Architectures and Compilation Techniques (PACT-2003*), New Orleans, LA, September 2003.
80. Brian Mestan and Mikko Lipasti, "Exploiting Partial Operand Knowledge," in *Proceedings of the 32nd IEEE International Conference on Parallel Processing (ICPP-32)*, Kaohsiung, Taiwan, October 2003.
81. Ilhyun Kim and Mikko Lipasti, "Half-Price Architecture," in *Proceedings of the 30th International Symposium on Computer Architecture (ISCA-30)*, Anaheim, CA, June 2003.
82. Madhusudanan Seshadri and Mikko Lipasti, "A Case for Vector Network Processors," In *Proceedings of Network Processor Conference West*, pp. 387-405, San Jose, CA, October 2002.
83. Kevin Lepak and Mikko Lipasti, "Temporally Silent Stores," In *Proceedings of the 10th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X)*, pp. 30-41, San Jose, CA, October 2002.
84. Harold W. Cain and Mikko Lipasti, "Verifying Sequential Consistency Using Vector Clocks," In *Proceedings of the 14th ACM Symposium on Parallel Algorithms and Architectures (SPAA '02) Revue*, pp. 153-154, Winnipeg, Manitoba, August 2002.
85. Jarrod Lewis, Bryan Black, and Mikko Lipasti, "Avoiding Initializing Misses to the Heap," In *Proceedings of the 29th International Symposium on Computer Architecture (ISCA-29)*, pp. 183-194, Anchorage, AL, May 2002.
86. Ilhyun Kim and Mikko Lipasti, "Implementing Optimizations at Decode Time," In *Proceedings of the 29th International Symposium on Computer Architecture (ISCA-29)*, pp. 221-232, Anchorage, AL, May 2002.
87. Eric Weglarz, Kewal K. Saluja, and Mikko H. Lipasti, "Minimizing Energy Consumption for High-Performance Processing," In *Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design*, pp. 199-206, Bangalore, India, January 2002.

88. Milo Martin, Daniel Sorin, Harold Cain, Mark Hill, and Mikko Lipasti, "Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing," In *Proceedings of the 34th International Symposium on Microarchitecture (MICRO-34)*, pp. 328-337, Austin, TX, Nov. 2001.
89. Harold Cain, Ravi Rajwar, Morris Marden, and Mikko Lipasti, "An Architectural Evaluation of Java TPC-W," in *Proceedings of the 7th International Symposium on High-Performance Computer Architecture (HPCA-7)*, pp. 229-240, Monterrey, Mexico, January 2001.
90. Kevin Lepak and Mikko Lipasti, "Silent Stores for Free," In *Proceedings of the 33rd International Symposium on Microarchitecture (MICRO-33)*, pp. 22-31, Monterey, CA, December 2000.
91. Gordon Bell, Kevin Lepak, and Mikko Lipasti, "A Characterization of Silent Stores," In *Proceedings of the 9th International ACM/IEEE Conference on Parallel Architectures and Compilation Techniques (PACT-2000*), Philadelphia, PA, October 2000.
92. Kevin Lepak and Mikko Lipasti, "On the Value Locality of Store Instructions," In *Proceedings of the 27th International Symposium on Computer Architecture (ISCA-27)*, pp. 182-191, Vancouver, B.C., June 2000.
93. Derek L. Howard and Mikko H. Lipasti, "The Effect of Program Optimization on Trace Cache Efficiency," *In Proceedings of the 8th International ACM/IEEE Conference on Parallel Architectures and Compilation Techniques (PACT-1999*), October 1999.
94. Mikko H. Lipasti and John Paul Shen, "The Performance Potential of Value and Dependence Prediction," In *Proceedings of the 3rd European Conference on Parallel Processing (EUROPAR-97*), Passau, Germany, August 1997.
95. Mikko H. Lipasti and John Paul Shen, "Exceeding the Dataflow Limit via Value Prediction," In *Proceedings of the 29th International Symposium on Microarchitecture (MICRO-29)*, Paris, December 1996.
96. Mikko H. Lipasti, Christopher P. Wilkerson, and John Paul Shen, "Value Locality and Load Value Prediction," In *Proceedings of the 7th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VII)*, Boston, October 1996.
97. Bryan Black, Andrew S. Huang, Mikko H. Lipasti, and John Paul Shen, "Can Trace-Driven Simulators Accurately Predict Superscalar Performance?" In *Proceedings of the IEEE International Conference on Computer Design (ICCD-96)*, San Antonio, Texas, October 1996.
98. Mikko H. Lipasti, William J. Schmidt, Robert R. Roediger, and Steven R. Kunkel, "SPAID: Software prefetching in pointer- and call-intensive environments," In *Proceedings of the 28th International Symposium on Microarchitecture (MICRO-28)*, Ann Arbor, Michigan, November 1995.
99. Trung A. Diep, Mikko H. Lipasti, and John P. Shen, "Architecture-Compatible Code Boosting for Performance Enhancement of the IBM RS/6000," In *Proceedings of the IEEE International Conference on Computer Design (ICCD-93)*, Boston, October 1993.

OTHER REFEREED PUBLICATIONS

100. Dibakar Gope and Mikko H. Lipasti, "Bias-Free Neural Predictor," in *Proceedings of 4th JILP Workshop on Computer Architecture Competitions (JWAC-4):Championship Branch Prediction (CBP-4)*, Minneapolis, MN, June 2014.
101. Amir Yazdanbakhsh, David Palframan, Azadeh Davoodi, Nam Sung Kim, and Mikko Lipasti, " Online and Operand-Aware Detection of Failures by Utilizing False Alarm Vectors," in *Proceeedings of 22nd International Workshop on Logic & Synthesis (IWLS),"* Austin, TX, June 2013.

102. Vignyan Reddy Kothinti Naresh, David J. Palframan and Mikko H. Lipasti, "Analyzing the Soft Error Resilience of the CRIB Microarchitecture," In *Proceedings of the 3rd Workshop on Resilient Architectures (WRA-3)*, Seattle, WA, December 2012.
103. Harold W. Cain and Mikko H. Lipasti, "Edge Chasing Delayed Consistency: Pushing the Limits of Weak Memory Models," in *Proceedings of the Workshop on Relaxing Synchronization for Multicore and Manycore Scalability (RACES'12)*, Tucson, AZ, October 2012 (archival publication via ACM Digital Library)
104. Mitchell Hayenga, Daniel Johnson, Mikko Lipasti, "Pitfalls of Orion-based Simulation," In *Proceedings of the Workshop on Duplicating, Deconstructing, and Debunking (WDDD-12)*, Portland, OR, June 2012.
105. David J. Palframan, Nam Sung Kim, and Mikko H. Lipasti , "Spare RIBs: Redundant Intermediate Bitslices," In *Proceedings of the 2nd Workshop on Resilient Architectures (WRA-2)*, Porto Alegre, Brazil, December 2011.
106. Guangyu Shi and Mikko H. Lipasti, "Perceptron Branch Prediction with Separated Taken/Not-Taken Weight Tables," in *Proceedings of the 2nd JILP Workshop on Computer Architecture Competitions: Championship Branch Prediction (JWAC-2)*, San Jose, CA, June 2011.
107. Mitchell Hayenga, Andrew T. Nere, and Mikko Lipasti, "MadCache: A PC-aware Cache Insertion Policy," *in Proceedings of the 1st JILP Workshop on Computer Architecture Competitions (JWAC-1): Cache Replacement Championship*, St. Malo, France, June 2010.
108. Andrew T. Nere and Mikko Lipasti, "Cortical Architectures on a GPGPU," in *Proceedings of the Third Workshop on General-Purpose Computation on Graphics Processing Units*, Pittsburgh, PA, March, 2010 (proceedings archived by ACM).
109. Eric Hill and Mikko Lipasti, "The Effect of Pipeline Depth on Logic Soft Errors," *in Proceedings of the 2010 IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE 2010)*, Stanford University, CA, March, 2010 (paper and poster presentation).
110. Eric Hill and Mikko Lipasti, "Logic Soft Errors in a Parallel CISC Decoder," *in Proceedings of the 2010 IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE 2010)*, Stanford University, CA, March, 2010 (paper and talk).
111. Karthik Jayaraman, Vivek Shrivastava, Brian Pellin, Martin Hock, and Mikko H. Lipasti, "Phase-based Adaptive Branch Predictor: Seeing the Forest for the Trees," In *Proceedings of the Workshop on Introspective Architecture (WISA)*, Austin, TX, February, 2006.
112. Pranay Koka and Mikko H. Lipasti, "Opportunities for Cache Friendly Process Scheduling," In *Proceedings of the Workshop on Interaction between Operating Systems and Computer Architecture (WIOSCA)*, October, 2005.
113. Erika Gunadi and Mikko H. Lipasti, 'Cache Pipelining with Partial Operand Knowledge," in *Proceedings of the Workshop on Complexity-Effective Design (WCED)*, Munich, Germany, June 2004.
114. Pranay Koka and Mikko Lipasti, "Characterization of an IMAP server on a Shared-Memory Multiprocessor," in *Proceedings of the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW '04)*, Madrid, Spain, February 2004.
115. Matt Ramsay, Chris Feucht, and Mikko H. Lipasti, "Exploring Efficient SMT Branch Predictor Design," In *Proceedings of the Workshop on Complexity-Effective Design (WCED)*, San Diego, CA, June 2003.
116. Harold W. Cain, Kevin M. Lepak, and Mikko H. Lipasti, "Precise and Accurate Processor Simulation," In *Proceedings of the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW)*, Boston, MA, February 2002.
117. Morris Marden, Shih-Lien Lu, Konrad Lai, and Mikko H. Lipasti, "Comparison of Memory System Behavior in Javan and Non-Java Commercial Workloads," In *Proceedings of*

the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW), Boston, MA, February 2002.

118. Craig Saldanha and Mikko H. Lipasti, "Power Efficient Cache Coherence," In *Proceedings of the Workshop on Memory Performance Issues (WMPI)*, Goteborg, Sweden, June 2001.

119. Jason F. Cantin, Mikko H. Lipasti, and James E. Smith, "Dynamic Verification of Cache Coherence Protocols," In *Proceedings of the Workshop on Memory Performance Issues (WMPI)*, Goteborg, Sweden, June 2001.

120. Harold Cain, Kevin Lepak, and Mikko Lipasti, "A Dynamic Binary Translation Approach to Architectural Simulation," In *Proceedings of the Workshop on Binary Translation (WBT)*, Philadelphia, PA, October 2000.

WORKSHOP PAPERS AND TECHNICAL REPORTS

121. Dibakar Gope and Mikko H. Lipasti, "Statement-Level Parallelism," in *Proceedings of the First Workshop on the High Performance Scripting Languages*, San Francisco, CA, February 2015.

122. Atif Hashmi, Andrew Nere, and Mikko H. Lipasti, "Learning through Spatially Localized and Temporally Correlated Spontaneous Activations," in *Proceedings of the 15th International Conference on Cognitive and Neural Systems (ICCNS)*, Boston, MA, May 2011 (abstract and talk).

123. Atif Hashmi and Mikko Lipasti, "Discovering Cortical Algorithms," In *Proceedings of 14th Int'l Conference on Cognitive and Neural Systems (ICCNS),* Boston, MA, May 2010 (abstract and talk).

124. Atif Hashmi, Hugues Berry, Olivier Temam, and Mikko Lipasti, "Leveraging Progress in Neurobiology for Computing Systems," In *Proceedings of the 1st Workshop on New Directions in Computer Architecture* (in conjunction with the 42nd 2009 International Symposium on Microarchitecture), New York, NY, December 2009.

125. Nathan Binkert, Al Davis, Mikko Lipasti, Robert Schreiber, and Dana Vantrease, "Nanophotonic Barriers," In *Proceedings of the 1st Workshop on Photonic Interconnects and Computer Architecture* (in conjunction with the 42nd 2009 International Symposium on Microarchitecture), New York, NY, December 2009.

126. Gordon B. Bell and Mikko H. Lipasti, "Profligate Execution," Technical Report, Department of Electrical and Computer Engineering, University of Wisconsin-Madison, September 2006. Available from http://www.ece.wisc.edu/~pharm.

127. Mikko H. Lipasti, "Value Locality and Speculative Execution," Ph.D. Thesis, Department of Electrical and Computer Engineering, Carnegie Mellon University, May 1997.

128. Bohuslav Rychlik, Mikko H. Lipasti, and John Paul Shen; "Experimental Characterization of Value Locality," Technical Report CMuART-1997-04, Department of Electrical and Computer Engineering, Carnegie Mellon University, 1997

129. Mikko H. Lipasti and John Paul Shen, "Approaching 10 IPC via Superspeculation," Technical Report CMU-MIG-97-1, Department of Electrical and Computer Engineering, Carnegie Mellon University, January 1997.

130. Mikko H. Lipasti, "Compilation Support for Superscalar Processors," M.S. Thesis, Department of Electrical and Computer Engineering, Carnegie Mellon University, December 1992.

131. Mikko H. Lipasti, "Cache Visualization," *IBM Technical Disclosure Bulletin,* vol. 38 no. 8, pp. 407-408, August 1995.

132. Mikko H. Lipasti and Arturo Martin-de-Nicolas, "Low-Cost Instruction and Address Tracing", *IBM Technical Disclosure Bulletin*, vol. 38 no. 8, pp. 309-310, August 1995.

133. Mikko H. Lipasti, "Compile-Time Elimination of Store-Fetch Interlock Delays," *IBM Technical Disclosure Bulletin,* vol. 37 no. 10, pp. 217-218, October 1994.

PATENT APPLICATIONS

134. David J. Palframan, Nam Sung Kim, and Mikko Lipasti, "Memory Fault Patching Using Pre-existing Memory Structures,", patent pending, filed October 2014.
135. Dibakar Gope and Mikko Lipastim "Apparatus and method for Bias-free Branch Prediction,"patent pending, filed June 2014.
136. David J. Palframan, Nam Sung Kim, and Mikko Lipasti, "Method and Apparatus for Soft error Mitigation in Computers," patent pending, filed February 2014.
137. Atif G. Hashmi, Andrew Nere, Mikko Lipasti, and Giulio Tononi, "Sensory Stream Analysis via Configurable Trigger Signature Detection," patent pending, filed January 2013.
138. Mikko H. Lipasti, "Memory access request reordering to reduce memory access latency," U.S. Patent number 6,487,640, issued Nov. 26, 2002.
139. Mikko H. Lipasti, "Data cache miss lookaside buffer and method thereof," U.S. Patent number 6,487,639, issued Nov. 6, 2002.
140. Mark R. Funk, Steven R. Kunkel, Mikko H. Lipasti, Bilha Mendelson, Robert R. Roediger, and William J. Schmidt., "Intelligent Cache Management Mechanism," U.S. Patent number 6,314,561, issued Nov. 6, 2001.
141. Mikko H. Lipasti, "Circuit Arrangement and Method of Dispatching Instructions to Multiple Execution Units," U.S. Patent number 6,219,780, issued April 17, 2001.
142. Keith V. Besaw, Robert J. Donovan, Patrick T. Haugen, Mark J. Hessler, Mikko H. Lipasti, and Robert R. Roediger, "Method and Apparatus for Enabling Global Compiler Optimization in the Presence of Exception Handlers within a Computer Program," U.S. Patent number 5,778,233, issued July 1998.
143. James L. Denton, Richard J. Eickemeyer, Kevin C. Griffin, Ross E. Johnson, Steven R. Kunkel, Mikko H. Lipasti, and Sandra K. Ryan, "System and method for increasing cache efficiency through optimized data allocation," U. S. Patent number 5,651,135, issued July 1997.
144. Steven R. Kunkel, et al., "Cache multi-block touch mechanism for object oriented computer system," patent pending, filed October 1996.

TEACHING EXPERIENCE

2009- Professor. University of Wisconsin, Madison, WI

Courses taught

Fall 2009	ECE 601 Mobile Computing Systems Laboratory
Spring 2010	ECE 752 Advanced Computer Architecture I
Fall 2010	ECE 552 Introduction to Computer Architecture
	ECE 252 Introduction to Computer Engineering
Spring 2011	ECE 352 Digital Systems Fundamentals
Summer 2011	Parallel Processing at NUDT Summer School, Changsha, China
Fall 2011	ECE 252 Introduction to Computer Engineering
Spring 2012	ECE 554 Digital Engineering Laboratory
	ECE 752 Advanced Computer Architecture I
Fall 2012	ECE 751 Embedded Computing Systems
Spring 2013	ECE 757 Advanced Computer Architecture II

	Spring 2014	ECE 554 Digital Engineering Laboratory
		ECE 901 Digital Systems Prototyping
	Spring 2015	ECE 757 Advanced Computer Architecture II
2005-2009	Associate Professor. University of Wisconsin, Madison, WI Courses taught	
	Fall 2005	ECE 352 Digital System Fundamentals
		ECE 552 Introduction to Computer Architecture
	Spring 2006	ECE 379 Introduction to Computer Engineering
	Fall 2007	ECE 252 Introduction to Computer Engineering
	Spring 2008	ECE 752 Advanced Computer Architecture I
	Fall 2008	ECE 252 Introduction to Computer Engineering
		ECE 601 Mobile Computing Systems Laboratory
	Spring 2009	ECE 757 Advanced Computer Architecture II
2005	Visiting Instructor, United States Patent and Trademark Office, Alexandria, VA	
	Taught a short course (3 + 2 days) covering advanced topics in processor architecture to the patent examiner art unit specializing in computer architecture.	
1999-2005	Assistant Professor. University of Wisconsin, Madison, WI Courses taught	
	Fall 1999	ECE 902 Commercial Servers and Workloads
	Spring 2000	ECE 752 Advanced Computer Architecture I
	Fall 2000	ECE 757 Advanced Computer Architecture II
	Spring 2001	ECE 554 Digital Engineering Laboratory
		ECE 752 Advanced Computer Architecture II
	Spring 2002	ECE 552 Introduction to Computer Architecture
	Fall 2002	ECE 554 Digital Engineering Laboratory
	Spring 2003	ECE 352 Digital System Fundamentals
	Fall 2003	ECE 752 Advanced Computer Architecture I
	Spring 2004	ECE 554 Digital Engineering Laboratory
	Spring 2005	ECE 554 Digital Engineering Laboratory
		ECE 752 Advanced Computer Architecture I
Spring 1998	Adjunct Faculty. University of Minnesota, Minneapolis, MN I taught an advanced graduate-level class on computer architecture that was offered through both the Electrical and Computer Engineering (ECE) and Computer Science and Engineering (CSE) departments to a combined enrollment of 40 students. Class research projects resulted in two conference paper submissions.	
1995-1997	Undergraduate Advisor. Carnegie Mellon University, Pittsburgh, PA As a Ph.D. candidate, I supervised the research projects of two undergraduate students, meeting with them regularly to advise them by setting realistic goals and helping them to attain these goals, culminating in the publication of a co-authored conference paper.	
Spring 1992	Teaching Assistant. Carnegie Mellon University, Pittsburgh, PA For the sophomore-level digital design course, I prepared and delivered a weekly recitation; helped prepare for and supervised digital design laboratory experiments and projects; and assisted with homework, quiz, and exam preparation and grading.	

Fall 1991 Teaching Assistant. Carnegie Mellon University, Pittsburgh, PA
I prepared and delivered lectures and assisted with homework, quizzes, and exams.

GRADUATE STUDENTS SUPERVISED

(AMD)	Kevin Lepak	M.S. 12/2000, Ph.D. 12/2003
(Intel)	Ilhyun Kim	M.S. 5/2001, Ph.D. 5/2004
(IBM, Qualcomm)	Harold Cain	Ph.D. 11/2004
(IBM, Qualcomm)	Jason Cantin	M.S. 12/2002, Ph.D. 5/2006 (co-advisor J.E. Smith)
(IBM, Qualcomm)	Gordon Bell	M.S. 5/2001, Ph.D. 12/2007
(Univ. of Toronto)	Natalie Enright Jerger	M.S. 5/2004, Ph.D. 2008
(Intel)	Eric Hill	M.S. 5/2004, Ph.D. 2008
(Intel, Qualcomm)	Lixin Su	Ph.D. 8/2008
(Qualcomm)	Dana Vantrease	Ph.D. 5/2010
(Intel, SMI)	Erika Gunadi	M.S. 5/2005, Ph.D. 5/2010
(Thalchemy)	Atif Gul Hashmi	M.S. 12/2007, Ph.D. 12/2011
(ARM Research)	Mitch Hayenga	Ph.D. 8/2013
(Thalchemy)	Andrew Nere	M.S. 12/2009, Ph.D. 5/2013
(NVidia)	Sean Franey	M.S. 5/2011, Ph.D. 8/2014
(Qualcomm)	Vignyan Kothinti Naresh	Ph.D. 8/2014
(NVidia Research)	Arslan Zulfiqar	Ph.D. 8/2014
(ARM Research)	David Palframan	M.S. 5/2011, Ph.D. 5/2015 (co-advisor N.S. Kim)
(AMD Research)	Sooraj Puthoor	M.S. 8/2012, Ph.D. (expected)
	Dibakar Gope	Ph.D. (expected)
	Michael Mishkin	Ph.D. (expected, co-advisor N.S. Kim)
	Gokul Ravi	Ph.D. (expected)
	Rohit Shukla	Ph.D. (expected)
	Essan Swain	M.S. 5/2015, Ph.D. (expected)
	David Schlais	M.S./Ph.D. (expected)
(Intel)	Morris Marden	M.S. 5/2001
(Intel, Amazon)	Craig Saldanha	M.S. 5/2001
(IBM, Apple)	Brian Mestan	M.S. 5/2002
(UT-Austin	Jarrod Lewis	M.S. 12/2002
(Intel)	Madhusudanan Seshadri	M.S. 5/2002
(Sun, Oracle)	Razvan Cheveresan	M.S. 8/2003
(Sun, AMD)	Matt Ramsay	M.S. 12/2003
(Sun, Oracle)	Pranay Koka	M.S. 12/2004
(Oracle, VMWare)	Ramya Narayana	M.S. 5/2004
(Intel)	Vaishali Karanth	M.S. 5/2010
(Oracle)	Guangyu Shi	M.S. 5/2011
(Qualcomm)	Mushfique Khurshid	M.S. 5/2013
(NVidia)	Abhishek Aggarwal	M.S. 5/2013

(Qualcomm)	Neal Haas	M.S. 2014 (co-advisor N.S. Kim)
(BAE)	Addison Floyd	M.S. 2015 (co-advisor N.S. Kim)
	Sriharsha Yerramalla	M.S. 5/2015
(Dallas Cowboys)	Travis Frederick	B.S. 5/2013
	Xiaoshen Zhang	B.S. 5/2016 (expected)
	Eric Jorgensen	B.S. 5/2016 (expected)

RESEARCH FUNDING

2015-2016	Qualcomm gift funds, $50,000
2015-2016	SEED Research Program Grant, $122,000
2014-2016	NSF SBIR Phase II, $609,394 (P.I. Atif Hashmi, Thalchemy Corp.)
2013-2016	NSF SHF, “Reliable In-place Execution for Multicore Processors,” $500,000
2013-2014	Qualcomm Research Award, $55,000
2013	Robert Draper Technology Innovation Fund, $50,000
2013	Innovation & Economic Development Research Program (IEDR), $50,000
2013	NSF SBIR Phase I, $150,000 (P.I. Atif Hashmi, awarded to Thalchemy Corp.)
2012-2013	Oracle Labs Research Award, $45,000
2012-2013	NSF Innovation Corps, $50,000
2008-2014	Philip Dunham Reed Chair, $35,000/year
2011-2012	Oracle Labs Research Award, $45,000
2011-2012	Google Faculty Research Award, $40,000
2011-2014	NSF SHF, “Arbitration, Coherence, and Consistency for Nanophotonics,” $430,000
2010-2011	NSF CPA Supplement, “Lazy Logic,” $60,000
2009-2010	HP Innovation Research Award, $75,000
2008-2009	HP Innovation Research Award, $75,000 + $35,000 in equipment
2008-2009	Nokia Research Award, $70,000
2008-2009	Intel Research Council Award, $35,000, *withheld due to WARF lawsuit*
2007-2008	Intel Research Council Award, $35,000 + $8,000 in equipment
2007-2010	NSF CPA, “Lazy Logic,” $300,000
2006-2007	Intel Research Council Award, $35,000
2006-2007	IBM Faculty Partnership Award, $30,000
2005-2006	Intel Research Council Award, $35,000
2004-2007	NSF CPA, “Collaborative Coherence,” $175,000
2004-2005	Intel Research Council Award, $35,000 + $6,000 in equipment
2003-2004	Intel Research Council Award, $35,000 + $6,000 in equipment
2003	Intel MRL Equipment donation, ~$60,000 for 100 CPUs and 50 motherboards
2003-2004	IBM Faculty Partnership Award, $40,000, *withheld due to pending WARF litigation*
2003	IBM Shared University Research equipment grant, ~$300,000, *also withheld*
2002-	Peter Schneider Computer Engineering Junior Faculty Fellowship, $25,000
2002	Xilinx University Program equipment donation, $244,295

2002-2003	Intel Research Council Award, $35,000 + $6,000 in equipment
2002-2007	NSF CAREER, “Semantic Decomposition of Instruction Sets,” $375,000
2001-2004	NSF NGS, “Wisconsin DOVE: Distributed Optimizing Virtual Environment,” Co-PI Rastislav Bodik, Andrea Arpaci-Dusseau, $600,000, 33% share
2001-2002	IBM Faculty Partnership Award, $40,000
2001-2002	Intel Research Council Award, $35,000 + $16,000 in equipment
2000-2003	NSF ITR, “Dynamic Verification of Parallel Distributed Systems,” Co-PI James Smith, $450,000, 50% share
2000-2003	NSF CISE, “Exploiting Value Locality in Shared-Memory Multiprocessors,” $250,000
2000	IBM Shared University Research grant, co-PI Ras Bodik, $500,000 in equipment
2000	Intel MRL Equipment donation, co-PI Chung-Ping Chen, $25,000 in equipment
2000-2001	Intel Research Council Award, $35,000 + $20,000 in equipment
2000-2001	IBM Faculty Partnership Award, $40,000
1999	IBM Shared University Research grant, $716,000 in equipment

PROFESSIONAL ACTIVITIES

ACM Transactions on Architecture and Code Optimization (TACO), Board of Distinguished Reviewers, 2014-

Co-editor, IEEE MICRO Special Issue on Systems for Very Large Scale Computing, 2011

IEEE MICRO Top Picks Program Committee: 2007, 2009, 2011

MICRO Program Co-chair: 2007

MICRO Program Committee: 2003, 2011

HPCA Program Committee: 2001, 2006, 2009, 2010, 2013, 2015

ISPASS Program Committee: 2004, 2005, 2006, 2008, 2009

ISCA Program Committee: 2004, 2005, 2010, 2012, 2013

NOCS Program Committee: 2012

PACT Program Committee: 2000, 2001

ICCD Program Committee: 2008, 2009

ICS (Int’l Conference on Supercomputing) Program Committee: 2003, 2014

CF (Computing Frontiers) Program Committee, 2014

ICPP Program Committee: 2001

Workshop on Duplicating, Deconstructing, and Debunking, co-organizer: 2002-2004

WDDD Program Committee: 2005-2009

WMPI Program Committee: 2006

Value Prediction Workshop Program Committee: 2003

Workshop on Optimizing Middleware Program Committee: 2001

ISCA Workshop Chair: 2005

PACT Tutorials Chair: 2001

Advised Hilldale Student/Faculty Undergraduate Research Award recipient, 2002-2003

Advised 2 undergraduates for SURE program in Summer 2000

Presenter for numerous conference publications

Invited speaker for various seminars

Member, IEEE and Tau Beta Pi

Panel member for NSF and DOE proposal review

Paper reviewer for numerous conferences and journals

University, College, and Departmental service:

- CAE Executive Committee, 2011-
- Curriculum Committee chair: 2005-2006, 2007-2008, 2008-2009, 2011-2013
- Fellowship committee: 1999-2002, 2004-2005
- College of Engineering Curriculum Committee (APCRC): 2005-2006, 2007-2010
- Graduate Admissions committee: 2004-2005
- Undergraduate advising committee: 2000-2009
- Faculty Recruiting committee: 2002 - 2005, 2010-2011
- Tenure and Promotion committee: 2009-2011, 2012-2015
- Awards Committee, 2013-2014
- Curriculum revision implementation committee: 2010-2011
- Advisor, AMEP degree program: Fall 2002-
- Byron Bird Award Selection Committee: 2002, 2005, 2006

PERSONAL

Male, born 4/9/1968, fluent in English and Finnish, dual citizenship (Finland/U.S.A.)

REFERENCES

Available on request.